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Implementation and testing of a 32-Bit LEON processor for On-Board Computers in Satellite Control Systems

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Abstract

The advances in VLSI technology leading to availability of high performance microprocessors, ASICs/FPGAs, high density memories and also improved packaging technology for space applications has made miniaturization possible in spacecraft electronics. Traditionally, attitude and orbit control, telecommand, telemetry, sensor electronics, thermal management etc., are generally implemented as stand-alone sub-systems. The feasibility of miniaturization in spacecraft electronics has led to the integration of the above systems into a single on-board computer system to realize the same functions. This paper presents an on-board computer (OBC) system also known as the spacecraft Bus Management unit (BMU). Environmental and other constrains which render satellite computers to be different from that of equivalent ground machines and realization of such a computer using a 32 bit LEON3FT processor which is to be designed for the spacecraft application. Mil STD 1553 Protocol is the one of the major protocol which has to be sustained to perform the interaction with various other peripheral devices in a satellite.

Keywords: LEON, SCS.

Introduction

Advances in semiconductor technologies have led to miniaturization in spacecraft electronics. This has made it possible to integrate many stand-alone electronic systems into a single unified system to realize the same / enhanced functional requirements. This minimizes the glue logic - protection circuitry, connectors, harness, cables etc., and also mechanical packaging. Thus, the design emphasis is now directed towards a sophisticated centralized information processing system and realization of spacecraft electronics with minimum power consumption, weight and volume. Cost-effective spacecraft engineering is achieved by integrating the various elements of the spacecraft bus that realize the following functions:

- Command processing
- Data acquisition and processing
- Attitude and Orbit control
- Telemetry and Housekeeping
- Thermal Management

into a single Spacecraft Bus Management Unit (BMU) which uses standard interfaces such as MIL-STD-1553B with rest of the spacecraft as shown in Figure 1. The use of standard interfaces between BMU and other systems will decrease the volume and mass of cabling and the associated connectors and simplifies integration in a spacecraft. It also results in unification of testing and reduces the turnaround time for delivery of BMUs for spacecraft realization.

The spacecraft BMU also improves the payload to spacecraft bus ratio. Additionally, as the number of satellites is increasing, spacecraft autonomy becomes important to minimize the load on ground support for day-to-day operations. Thus, the design of the BMU is governed by the following factors:

• Compact realization at package level
• Minimal interfaces at spacecraft level
• Operational consideration at mission level.

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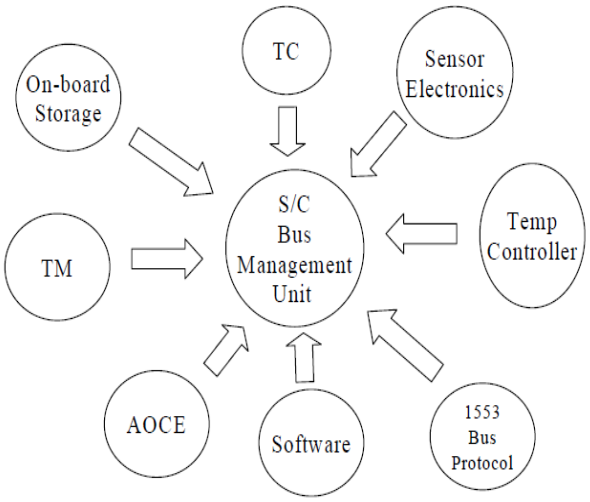

Figure 1: Integration of stand-alone sub-systems into S/C bus management unit

The BMU framework can be appropriately scaled to meet the mission requirements of various classes of satellites design.

Evolution of OBC

OBC (ON BOARD COMPUTER) was basically designed to control the Attitude controlling within the satellite when placed in Orbit. But later due to advancement in technology the necessity of improving the OBC have become a critical issue. Today OBC have been interconnected with various other Packages/Payloads to control various operations within the satellite. To perform this operation we make use of MIL STD 1553B Protocol to perform the communication. Functions such as Telecommand, Telemetry, Automated onboard control system, Sensor Electronics can be integrated in the BMU framework and facilitate mission operations to be carried out with minimum ground support. The use of high density connectors, surface mount packaging for new HMCs, Extensive hybridization (Solid state switch, IB, OB, RC networks, Line filters), analog ASIC based Relay Drivers, high density PROMS / SRAMS, Passive chip components, improved packaging for double side mounting of components, high density FPGA based digital logic realization, MIL-Std-1553B interface to reduce spacecraft level harness & functional distribution / realization of logics have been a major step in the transition from second generation distributed sub-systems to the third generation BMU frame-work based spacecraft engineering. In view of the criticality of RH1280 device and additional experience gained from the development & testing of FPGA BMU, the next generation ASIC based OBC is being developed with enhanced capabilities.

Basic Constraints

The reliability requirement for the on board the satellite have to be enhanced. The global reflect on the basic of an On Board Computer in the following way:

- The intrinsic mass of the computer must be low.
- The power consumption must be minimized, since the masses of the solar array and batteries are roughly proportional to the electrical energy to be generated or stored.
- The volume of the computer should be reasonable for its mass.
- The Reliability of the computer must be exceptionally high.

The Space Environment

The space environment plays an important role in determining the characteristics of a satellite computer.

The first demand on the endurance of the space borne equipment occurs during the launch when it is subjected only to quite strong acceleration but also to a considerable amount of vibration which is generated by the vehicle during the launch.

Although the launch persists only for a small duration of time, the equipment is subjected to a great stress during this time and must be designed to withstand this stress.

Space itself is notable for being more or less a vacuum. Additionally solar energy will be incident on the spacecraft. While some of this energy is converted into electrical energy by the solar array, the rest will be absorbed by the spacecraft itself. Convention cooling is not possible and a combination of conduction and radiation cooling must be used to cool the spacecraft. If the spacecraft goes in and out of eclipse frequently it will be subjected to thermal cycling. For these reasons equipment having a low power consumption is favored since it reduces the likelihood of 'hotspots' which causes premature failures, and designs must be able to withstand the effects of thermal cycling.

Although space is regarded as a vacuum, it nevertheless contains the considerable quantities of energetic charged particles. Various levels of such radiation can have a damaging effect on semiconductor devices and degrade their performances under certain circumstances.

Reliability

Good Reliability can be achieved by two projected approaches. The first of this pronged approach involves careful manufacture of all parts, supported by good inspection and quality control.

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This activity involves not only visual inspection but also the use of highly sophisticated equipments to be involved in the inspection. Most high reliability components carry with them a good deal of documentation which outlines the life history of the component and the test which it has undergone. In this way the defective batches can be easily traced at any time.

The second pronged approach is in the design of the system and the hardware itself. By first keeping the system as simple as possible a good deal of potential problems are avoided. System reliability can be further enhanced by introducing further redundant circuitry which will take over the further function of the circuit which has failed.

Redundancy may be in two forms:

- Masking redundancy :

  In this case identical units operate continuously in parallel. A voting circuit computes the majority vote and ignore the output of the dissenting unit.
- Stand by Redundancy :

  Any one of the unit operates at a time depending upon which has been chosen by the switch, while the other units standby unpowered.

To summarize the trade-off between the two techniques stand by redundancy offers longer life, but service will be interrupted in case of failure. Masking redundancy offers continued service but over a shorter overall lifetime.

Operational Requirements

The functions performed by a satellite computer may be likened to certain extent to those performed by a small process control computer.

The computer is connected to various satellite subsystems or experiments which provide raw or pre-processed data. Some of these systems may be controlled by computers in a closed loop systems, where as others simply produce data which should be processed prior to being sent to ground.

Communication between round and satellite will be over the normal satellite telecommand and telemetry links. The capacity of these links is weak compared to what is possible on ground mainly due to limitations which must be imposed on the design of the on board antenna and transmitter. Because of the use of error detecting codes and synchronization words the rate of basic information transfer is considerably less, of the order one quarter. A wider range of possibilities exists for down link where it depends upon the characteristics of the On-Board communications package and mission. Format efficiency of 90% is typical and a great deal of the capacity of a down link can be used to carry information.

The telecommand up link can be used for sending on/off commands to the computer and for reprogramming the memory during the flight. This is a highly desirable feature to have, since it greatly adds to the flexibility of the machine, but it introduces problems of ensuring that the memory data is correctly received and loaded in to the correct address. Programs should occupy s little memory space as possible since this not only reduces the weight of the flight memory, but also reduces the time needed to load a program.

If the computer should fail, we must be able to diagnose the fault from the ground by way of existing radio links. Simple instruction test routines are always not enough. The diagnostic information must be sufficient to pin point the fault with some degree of accuracy in case in-flight reconfiguration of the computer might restore it run in degraded mode. It is also useful to perform in flight diagnostic in a routine manner at regular intervals and telemeter the results to the ground and establish confidence in the computer.

Proposed System

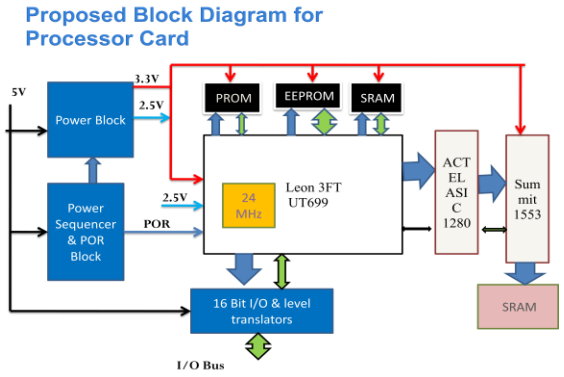

Figure2: Block Diagram of OBC

Computation need is increasing in our day to day life; so in the proposed Diagram we are implementing an LEON3FT processor which is of 32 bit in size and is made to process at 24 MHz. This operating frequency is twice as that of the previous module thereby improving the processing speed of the device in improving the MIPS rate leading to an accelerated speed in the execution of data. Here we also make use of the Actel's AX2000 FPGA which is used for simulation of the entire design using equivalent FPGA IP cores to improve more on the execution speed.

The basic requirements of the processor to communicate are the Memory devices where we make use of SRAM, PROM and EEPROM. All these

memory devices consume 3.3V only for their operation which helps in reduced power consumption thereby improving the lifetime of the battery.

Here we make use of the Power Block, Power Sequencer & POR Block. The Power block provides the several power supplies required for the demand from multiple sources within the circuitry. The power sequencer is user to regulate the power supply which for instance, in the case of satellites wherein the most commonly used is the solar panels during eclipse or during the shadow time's shortage of solar power is observed during such situations battery backup should be used to resolve such problem for which the power sequencer takes control of such applications where it switches to battery mode or to the solar conversion modes.

The POR block is used for resetting the device upon on provision to the supply to the controller. This is used basically to reset the device upon the beginning stages of the satellite when the program begins it execution.

The SRAM is used for temporarily storing the data and reading the data upon the execution of the program for real time applications.

The PROM and EEPROM are used for permanently stored data where upon resetting the device these memory devices loads the data into the SRAM for executing the initial stages of the program for real time program execution.

RTEMS (RTOS)

RTEMS (**R**eal-**T**ime **E**xecutive for **M**ultiprocessor **S**ystems) is a free open source real-time operating system (RTOS) designed for embedded systems. RTEMS is designed to support various open API standards including POSIX and uITRON. The API now known as the Classic RTEMS API was originally based upon the Real-Time Executive Interface Definition (RTEID) specification. RTEMS includes a port of the FreeBSD TCP/IP stack as well as support for various file systems including NFS and the FAT file system.

RTEMS does not provide any form of memory management or processes. In POSIX terminology, it implements a single process, multithreaded environment. This is reflected in the fact that RTEMS provides nearly all POSIX services other than those which are related to memory mapping, process forking, or shared memory. RTEMS closely corresponds to POSIX Profile 52 which is "single process, threads, file system".

RTEMS is used in many application domains. The EPICS community includes multiple people who are active RTEMS submitters. RTEMS is also popular for space uses since it supports multiple microprocessors developed for use in space including SPARC, ERC32 and LEON, MIPS Mongoose-V, Coldfire, and PowerPC architectures, which are available in space hardened models. It is used as the default operating system on the Milkymist Video Synthesizer.

Conclusion

Any project is incomplete without the desired results being fully achieved. The same stands in ours too. In our project we were required to create an On-Board Computer for communication with a MIL-STD- 1553 B bus, with an onboard RAM

After extensive testing and a few tweaks in the final PCB, we found that the designed Board fulfilled all the requirements to our satisfaction. The simulated results can be seen above in the form of timing diagrams. The On-Board Card also performs very well in its real time environment.. The card was found to be working in all the three cases namely:

1. Processor accessing the summit for programming it.
2. Processor accessing the On Board RAM for data stored in the RAM by the Summit.
3. Summit accessing the RAM to store the data which it receives from the MIL-STD-1553B Bus.

The On-Board system is used in the satellite system for communicating between subsystems. It fulfils all the requirements and can be used directly by incorporating the final changes that were made to it.

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